iC-NQC
13-bit Sin/D CONVERTER WITH SIGNAL CALIBRATION

FEATURES

♦ Resolution of up to 8,192 angle steps per sine period
♦ Binary and decimal resolution settings, e.g. 500, 512, 1000, 1024; programmable angle hysteresis
♦ Count-safe vector follower principle, real-time system with 70 MHz sampling rate
♦ Conversion time of just 250 ns including amplifier settling
♦ Input frequency of up to 250 kHz
♦ Direct sensor connection; selectable input gain
♦ Signal conditioning for offset, amplitude and phase
♦ A/B quadrature signals of up to 3.75 MHz with adjustable minimum transition distance
♦ Zero signal processing, adjustable in index position and width
♦ Absolute angle output via fast serial interface (BiSS, SSI)
♦ Period counting with up to 24 bits
♦ Error monitoring of frequency, amplitude and configuration
♦ Device setup from serial EEPROM or using BiSS
♦ ESD protection and TTL-/CMOS-compatible outputs

APPLICATIONS

♦ Interpolator IC for angle resolution from sine/cosine sensor signals
♦ Optical encoders
♦ MR sensor systems

PACKAGES

TSSOP20

BLOCK DIAGRAM
### DESCRIPTION

**iC-NQC** is a monolithic A/D converter which, by applying a count-safe vector follower principle, converts sine/cosine sensor signals with a selectable resolution and hysteresis into angle position data.

This absolute value is output via a bidirectional, synchronous-serial I/O interface in BiSS C protocol and trails a master clock rate of up to 10 Mbit/s. Alternatively, this value can be output so that it is compatible with SSI in Gray or binary code, with or without error bits. The device also supports double transmission in SSI ring mode.

Signal periods are logged quickly by a 24-bit period counter that can supplement the output data with an upstream multiturn position value.

At the same time any changes in angle are converted into incremental A QUAD B signals. Here, the minimum transition distance can be stipulated and adapted to suit the system on hand (cable length, external counter). A synchronized zero index Z is generated if enabled by PZERO and NZERO.

The front-end amplifiers are configured as instrumentation amplifiers, permitting sensor bridges to be directly connected without the need for external resistors. Various programmable D/A converters are available for the conditioning of sine/cosine sensor signals with regard to offset, amplitude ratio and phase errors (offset compensation by 8-bit DAC, gain ratio by 5-bit DAC, phase compensation by 6-bit DAC).

The front-end gain can be set in stages graded to suit all common complementary sensor signals from approximately 20 mVpp to 1.5 Vpp and also non-complementary sensor signals from 40 mVpp to 3 Vpp respectively.

The device can be configured using two bidirectional interfaces, the EEPROM interface from a serial EEPROM with I²C interface, or the I/O interface in BiSS C protocol. Free storage space on the EEPROM can be accessed via BiSS for the storage of additional data.

After a low voltage reset, iC-NQC reads in the configuration data including the check sum (CRC) from the EEPROM and repeats the process if a CRC error is detected.

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The device described here is a multifunctional IC that contains integrated BiSS C interface components. The BiSS C process is protected by patent DE 10310622 B4 owned by iC-Haus GmbH and its application requires the conclusion of a license (free of charge). Download the license at www.biss-interface.com/bua
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PACKAGING INFORMATION TSSOP20 (according to JEDEC Standard)

PIN CONFIGURATION
TSSOP20 4.4 mm, lead pitch 0.65 mm

PIN FUNCTIONS

<table>
<thead>
<tr>
<th>No.</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PCOS</td>
<td>Input Cosine +</td>
</tr>
<tr>
<td>2</td>
<td>NCOS</td>
<td>Input Cosine -</td>
</tr>
<tr>
<td>3</td>
<td>VDDA</td>
<td>+5 V Supply Voltage (analog) ¹)</td>
</tr>
<tr>
<td>4</td>
<td>GNDA</td>
<td>Ground (analog) ¹)</td>
</tr>
<tr>
<td>5</td>
<td>VREF</td>
<td>Reference Voltage Output</td>
</tr>
<tr>
<td>6 A</td>
<td>Incremental Output A</td>
<td>Analog signal COS+ (TMA mode)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PWM signal for Offset Sine (calib.)</td>
</tr>
<tr>
<td>7 B</td>
<td>Incremental Output B</td>
<td>Analog signal COS- (TMA mode)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PWM signal for Offset Cosine (calib.)</td>
</tr>
<tr>
<td>8 Z</td>
<td>Incremental Output Z</td>
<td>PWM signal for Phase/Ratio (calib.)</td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>10</td>
<td>VDD</td>
<td>+5 V Supply Voltage (digital)</td>
</tr>
<tr>
<td>11</td>
<td>SLI</td>
<td>I/O Interface, data input ²)</td>
</tr>
<tr>
<td>12</td>
<td>MA</td>
<td>I/O Interface, clock line</td>
</tr>
<tr>
<td>13</td>
<td>SLO</td>
<td>I/O Interface, data output</td>
</tr>
<tr>
<td>14</td>
<td>SDA</td>
<td>EEPROM interface, data line</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Analog signal SIN+ (TMA mode)</td>
</tr>
<tr>
<td>15</td>
<td>SCL</td>
<td>EEPROM interface, clock line ³)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Analog signal SIN- (TMA mode)</td>
</tr>
<tr>
<td>16</td>
<td>NERR</td>
<td>Error Input/Output, active low</td>
</tr>
<tr>
<td>17</td>
<td>PZERO</td>
<td>Input Zero Signal +</td>
</tr>
<tr>
<td>18</td>
<td>NZERO</td>
<td>Input Zero Signal -</td>
</tr>
<tr>
<td>19</td>
<td>PSIN</td>
<td>Input Sine +</td>
</tr>
<tr>
<td>20</td>
<td>NSIN</td>
<td>Input Sine -</td>
</tr>
</tbody>
</table>

¹) External connections linking VDDA to VDD and GND to GNDA are required.
²) If only a single iC-NQC is used and no chain circuitry of multiple BiSS slaves, pin SLI can remain unwired or can be linked to ground (GND).
³) It is not permissible to pull down pin SCL during power-up.
### ABSOLUTE MAXIMUM RATINGS

These ratings do not imply permissible operating conditions; functional operation is not guaranteed. Exceeding these ratings may damage the device.

<table>
<thead>
<tr>
<th>Item No.</th>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>G001</td>
<td>VDDA</td>
<td>Voltage at VDDA</td>
<td></td>
<td>-0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>G002</td>
<td>VDD</td>
<td>Voltage at VDD</td>
<td></td>
<td>-0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>G003</td>
<td>Vpin()</td>
<td>Voltage at PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, VREF, NERR, SCL, SDA, MA, SLI, SLO, A, B, Z</td>
<td>( V(i) &lt; VDDA + 0.3 \text{ V} ) ( V(i) &lt; VDD + 0.3 \text{ V} )</td>
<td>-0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>G004</td>
<td>Imx(VDDA)</td>
<td>Current in VDDA</td>
<td></td>
<td>-50</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td>G005</td>
<td>Imx(GNDA)</td>
<td>Current in GNDA</td>
<td></td>
<td>-50</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td>G006</td>
<td>Imx(VDD)</td>
<td>Current in VDD</td>
<td></td>
<td>-50</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td>G007</td>
<td>Imx(GND)</td>
<td>Current in GND</td>
<td></td>
<td>-50</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td>G008</td>
<td>Imx()</td>
<td>Current in PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, VREF, NERR, SCL, SDA, MA, SLI, SLO, A, B, Z</td>
<td></td>
<td>-10</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>G009</td>
<td>Ilu()</td>
<td>Pulse Current in all pins (Latch-up Strength)</td>
<td>according to Jedec Standard No. 78; ( Ta = 25^\circ \text{C} ); pulse duration to 10 ms; ( VDDA = VDDA_{\text{max}}, VDD = VDD_{\text{max}} ); ( Vlu() = (-0.5...+1.5) \times Vpin()_{\text{max}} )</td>
<td>-100</td>
<td>100</td>
<td>mA</td>
</tr>
<tr>
<td>G010</td>
<td>Vd()</td>
<td>ESD Susceptibility at all pins</td>
<td>HBM 100 pF discharged through 1.5 k( \Omega )</td>
<td></td>
<td>2</td>
<td>kV</td>
</tr>
<tr>
<td>G011</td>
<td>Tj</td>
<td>Junction Temperature</td>
<td></td>
<td>-40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>G012</td>
<td>Ts</td>
<td>Storage Temperature Range</td>
<td></td>
<td>-40</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

### THERMAL DATA

Operating Conditions: \( VDDA = VDD = 5 \text{ V} \pm 10 \% \)

<table>
<thead>
<tr>
<th>Item No.</th>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>T01</td>
<td>Ta</td>
<td>Operating Ambient Temperature Range (extended temperature range of -40 to 125 °C available on request)</td>
<td></td>
<td>-25</td>
<td>85</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.
### ELECTRICAL CHARACTERISTICS

Operating Conditions: $V_{DDA} = V_{DD} = 5 \, V \pm 10 \%$, $T_j = -40 \ldots 125 \, ^{\circ}C$, unless otherwise stated.

<table>
<thead>
<tr>
<th>Item No.</th>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
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<tr>
<td>001</td>
<td>$V_{DDA}$, $V_{DD}$</td>
<td>Permissible Supply Voltage</td>
<td></td>
<td>4.5</td>
<td>5.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>002</td>
<td>$I(V_{DDA})$</td>
<td>Supply Current in $V_{DDA}$</td>
<td>$f_{in} = 200 , kHz$; A, B, Z open</td>
<td>15</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>003</td>
<td>$I(V_{DD})$</td>
<td>Supply Current in $V_{DD}$</td>
<td>$f_{in} = 200 , kHz$; A, B, Z open</td>
<td>20</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>004</td>
<td>$V_{on}$</td>
<td>Turn-on Threshold $V_{DDA}$, $V_{DD}$</td>
<td></td>
<td>3.2</td>
<td>4.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>005</td>
<td>$V_{hys}$</td>
<td>Turn-on Threshold Hysteresis</td>
<td></td>
<td>200</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>006</td>
<td>$V_{c(\text{hi})}$</td>
<td>Clamp Voltage $\text{hi}$ at $\text{PSIN}$, $\text{NSIN}$, $\text{PCOS}$, $\text{NCOS}$, $\text{PZERO}$, $\text{NZERO}$, $V_{REF}$</td>
<td>$V_{c(\text{hi})} = V_{(\text{i})} - V_{DDA}$; $V_{c(\text{hi})} = V_{(\text{i})}$, other pins open</td>
<td>0.3</td>
<td>1.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>007</td>
<td>$V_{c(\text{lo})}$</td>
<td>Clamp Voltage $\text{lo}$ at $\text{PSIN}$, $\text{NSIN}$, $\text{PCOS}$, $\text{NCOS}$, $\text{PZERO}$, $\text{NZERO}$, $V_{REF}$, $\text{NERR}$, $\text{SCL}$, $\text{SDA}$, $\text{MA}$, $\text{SLI}$, $\text{SLO}$, A, B, Z</td>
<td>$I_{(\text{i})} = -1 , mA$, other pins open</td>
<td>-1.6</td>
<td>-0.3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>008</td>
<td>$V_{c(\text{hi})}$</td>
<td>Clamp Voltage $\text{hi}$ at $\text{NERR}$, $\text{SCL}$, $\text{SDA}$, $\text{MA}$, $\text{SLI}$, $\text{SLO}$, A, B, Z</td>
<td>$V_{c(\text{hi})} = V_{(\text{i})} - V_{DD}$; $V_{c(\text{hi})} = V_{(\text{i})}$, other pins open</td>
<td>0.3</td>
<td>1.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>101</td>
<td>$V_{os(\text{i})}$</td>
<td>Input Offset Voltage</td>
<td>$V_{in(\text{i})}$ and $G_{(\text{i})}$ in accordance with table $GAIN$; $G \geq 20$</td>
<td>-10</td>
<td>-15</td>
<td>15</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$G &lt; 20$</td>
<td></td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>102</td>
<td>$TC_{os}$</td>
<td>Input Offset Voltage</td>
<td>Temperature Drift</td>
<td></td>
<td></td>
<td></td>
<td>$\mu$V/K</td>
</tr>
<tr>
<td>103</td>
<td>$I_{in(\text{i})}$</td>
<td>Input Current</td>
<td>$V_{(\text{i})} = 0 , V \ldots V_{DDA}$</td>
<td>-50</td>
<td></td>
<td>50</td>
<td>nA</td>
</tr>
<tr>
<td>104</td>
<td>$G_{A}$</td>
<td>Gain Accuracy</td>
<td>$G_{(\text{i})}$ in accordance with table $GAIN$</td>
<td>95</td>
<td></td>
<td>102</td>
<td>%</td>
</tr>
<tr>
<td>105</td>
<td>$G_{Arel}$</td>
<td>Gain $\text{SIN}/\text{COS}$ Ratio Accuracy</td>
<td>$G_{(\text{i})}$ in accordance with table $GAIN$</td>
<td>97</td>
<td></td>
<td>103</td>
<td>%</td>
</tr>
<tr>
<td>106</td>
<td>$f_{hc}$</td>
<td>Cut-off Frequency</td>
<td></td>
<td>150</td>
<td>630</td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>107</td>
<td>$SR$</td>
<td>Slew Rate</td>
<td>$G = 80$</td>
<td>2.3</td>
<td></td>
<td>8.0</td>
<td>V/µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$G = 2.667$</td>
<td></td>
<td></td>
<td></td>
<td>V/µs</td>
</tr>
<tr>
<td>201</td>
<td>$AA_{abs}$</td>
<td>Absolute Angle Accuracy without calibration</td>
<td>referred to $360^\circ$ input signal, $G = 2.667$, $V_{in} = 1.5 , Vpp$, $HYS = 0$</td>
<td>-1.0</td>
<td></td>
<td>1.0</td>
<td>DEG</td>
</tr>
<tr>
<td>202</td>
<td>$AA_{abs}$</td>
<td>Absolute Angle Accuracy after calibration</td>
<td>referred to $360^\circ$ input signal, $HYS = 0$, internal signal amplitude of $2...4 , Vpp$</td>
<td>-0.5</td>
<td></td>
<td>$\pm 0.35$</td>
<td>+0.5</td>
</tr>
<tr>
<td>203</td>
<td>$AA_{rel}$</td>
<td>Relative Angle Accuracy</td>
<td>referred to signal periods at A, resp. B (see Fig. 1); $G = 2.667$, $V_{in} = 1.5 , Vpp$, $SELRES = 1024$, $FCTR = 0x0004 \ldots 0x00FF$, $fin &lt; fin_{max}$ (see table 15)</td>
<td>-10</td>
<td></td>
<td>10</td>
<td>%</td>
</tr>
<tr>
<td>801</td>
<td>$V_{REF}$</td>
<td>Reference Voltage</td>
<td>$I(V_{REF}) = -1 , mA \ldots +1 , mA$</td>
<td>48</td>
<td></td>
<td>52</td>
<td>% $V_{DDA}$</td>
</tr>
<tr>
<td>A02</td>
<td>$f_{osc(\text{i})}$</td>
<td>Oscillator Frequency</td>
<td>presented at pin $SCL$ with subdivision of $2048$; $V_{DDA} = V_{DD} = 5 , V \pm 10 %$</td>
<td>56</td>
<td>60</td>
<td>74</td>
<td>92</td>
</tr>
<tr>
<td>A03</td>
<td>$TC_{osc}$</td>
<td>Oscillator Frequency Temperature Drift</td>
<td>$V_{DDA} = V_{DD} = 5 , V$</td>
<td>-0.1</td>
<td></td>
<td></td>
<td>%/K</td>
</tr>
<tr>
<td>A04</td>
<td>$VC_{osc}$</td>
<td>Oscillator Frequency Power Supply Dependence</td>
<td></td>
<td>+9</td>
<td></td>
<td></td>
<td>%/V</td>
</tr>
</tbody>
</table>
### ELECTRICAL CHARACTERISTICS

Operating Conditions: VDDA = VDD = 5 V ±10 %, Tj = -40 ... 125 °C, unless otherwise stated.

<table>
<thead>
<tr>
<th>Item No.</th>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>B01</td>
<td>Vos()</td>
<td>Input Offset Voltage</td>
<td>V() = Vcm()</td>
<td>-20</td>
<td>20</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>B02</td>
<td>Iin()</td>
<td>Input Current</td>
<td>V() = 0 V ... VDDA</td>
<td>-50</td>
<td>50</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>B03</td>
<td>Vcm()</td>
<td>Common-Mode Input Voltage Range</td>
<td></td>
<td>1.4</td>
<td>VDDA-1.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>B04</td>
<td>Vdm()</td>
<td>Differential Input Voltage Range</td>
<td></td>
<td>0</td>
<td>VDDA</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

#### Incremental Outputs A, B, Z and I/O Interface Output SLO

| D01      | Vs(hi) | Saturation Voltage hi | Vs(hi) = VDD - V(); I() = -4 mA | 0.4  | V   |
| D02      | Vs(lo) | Saturation Voltage lo | I() = 4 mA | 0.4  | V   |
| D03      | tr()   | Rise Time | CL() = 50 pF | 60   | ns  |
| D04      | tf()   | Fall Time | CL() = 50 pF | 60   | ns  |
| D05      | RL()   | Permissible Load at A, B | TMA = 1 (calibration mode) | 1    | MΩ  |

#### I/O Interface Inputs MA, SLI

| E01      | Vt(hi) | Threshold Voltage hi | | 2   | V   |
| E02      | Vt(lo) | Threshold Voltage lo | | 0.8 | V   |
| E03      | Vt(hys) | Hysteresis | Vt(hys) = Vt(hi) - Vt(lo) | 300  | mV  |
| E04      | Ipu(MA) | Pull-up Current in MA | V() = 0 ... VDD - 1 V | -240 | -120 | -25  | µA   |
| E05      | Ipd(SLI) | Pull-down Current in SLI | V() = 1 ... VDD | 20   | 120  | 300  | µA   |
| E06      | fclk(MA) | Permissible MA Clock Frequency | SSI protocol | 4    | MHz |
| E07      | tp(MA-SLO) | Propagation Delay: MA edge vs. SLO output | RL(SLO) ≥ 1 kΩ | 10   | 50   | ns   |
| E08      | tbusy_s | Processing Time Single-Cycle Data (delay of start bit) | | 0   | µs  |
| E09      | tbusy_r | Processing Time Register Access (delay of start bit) | with read access to EEPROM | 2   | ms  |
| E10      | tidle | Interface Blocking Time | powering up with no EEPROM | 1   | 1.5  | ms   |
| E11      | t_tos | Timeout | TIM0 = 0, TOA=0 | 20   | µs  |

#### EEPROM Interface Inputs SDA and Error Input NERR

| F01      | Vt(hi) | Threshold Voltage hi | | 2   | V   |
| F02      | Vt(lo) | Threshold Voltage lo | | 0.8 | V   |
| F03      | Vt(hys) | Hysteresis | Vt(hys) = Vt(hi) - Vt(lo) | 300  | mV  |
| F04      | tbusya_cfg | Duration of Startup Configuration | error free EEPROM access | 5   | 7   | ms   |

#### EEPROM Interface Outputs SDA, SCL and Error Output NERR

| G01      | f()   | Write/Read Clock at SCL | | 20  | 100  | kHz |
| G02      | Vs()  | Saturation Voltage lo | I() = 4 mA | 0.45 | V   |
| G03      | Ipu() | Pull-up Current | V() = 0 ... VDD - 1 V | -600 | -300 | -75  | µA   |
| G04      | f()   | Fall Time | CL() = 50 pF | 60   | ns  |
| G05      | tmin() | Min. Duration Of Error Indication at NERR (lo signal) | MA = hi, no BiSS access, amplitude or frequency error | 10  | ms  |
| G06      | Tpwm() | Cycle Duration Of Error Indication at NERR | fosc() subdivided 2^2 | 60.7 | ms  |
| G07      | f()   | Duty Cycle Of Error Indication at NERR | signal duration low to high; AERR = 0 (amplitude error) FERR = 0 (frequency error) | 75   | 50   | %   |
| G08      | RL()  | Permissible Load at SDA, SCL | TMA = 1 (calibration mode) | 1   | MΩ  |
# ELECTRICAL CHARACTERISTICS

Operating Conditions: VDDA = VDD = 5 V ±10 %, Tj = -40...125 °C, unless otherwise stated.

<table>
<thead>
<tr>
<th>Item No.</th>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>H01</td>
<td>Vth</td>
<td>Voltage Threshold for Monitoring of Minimal Amplitude</td>
<td>VDDA = 5 V, SELAMPL = 0, AMPL = 0x00, PHI: 0°, 90°, 180°, 270°</td>
<td>2.8</td>
<td>3.0</td>
<td>3.2</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.0</td>
<td>3.2</td>
<td>3.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.2</td>
<td>3.4</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.4</td>
<td>3.6</td>
<td>3.8</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.0</td>
<td>3.2</td>
<td>3.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.2</td>
<td>3.4</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.4</td>
<td>3.6</td>
<td>3.8</td>
<td>V</td>
</tr>
<tr>
<td>H02</td>
<td>Vthmax</td>
<td>Upper Voltage Threshold for Monitoring of Sin²+Cos²</td>
<td>VDDA = 5 V, SELAMPL = 1, AMPL = 0x04...0x07, PHI: 0°, 45°...315°</td>
<td>3.35</td>
<td>4.5</td>
<td>4.95</td>
<td>V</td>
</tr>
<tr>
<td>H03</td>
<td>Vthmin</td>
<td>Lower Voltage Threshold for Monitoring of Sin²+Cos²</td>
<td>VDDA = 5 V, SELAMPL = 1, AMPL = 0x04, PHI: 0°, 45°...315°</td>
<td>0.2</td>
<td>1.0</td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.6</td>
<td>1.5</td>
<td>2.0</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.1</td>
<td>2.0</td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.6</td>
<td>2.5</td>
<td>3.0</td>
<td>V</td>
</tr>
</tbody>
</table>

**CHARACTERISTICS: Diagrams**

![Diagram](Figure 1: Definition of relative angle error and minimum transition distance)

![Diagram](Figure 2: Typical residual absolute angle error after calibration)
OPERATING REQUIREMENTS: I/O Interface

Operating Conditions: VDD = 5 V ±10 %, Ta = -25 ... 85 °C; input levels lo = 0 ... 0.45 V, hi = 2.4 V ... VDD

<table>
<thead>
<tr>
<th>Item No.</th>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Fig.</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSI Protocol</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1001</td>
<td>t_MAS</td>
<td>Permissible Clock Period</td>
<td>t_{los} according to Table 44</td>
<td>4</td>
<td>250</td>
<td>2x t_{los} ns</td>
<td></td>
</tr>
<tr>
<td>1002</td>
<td>t_MASH</td>
<td>Clock Signal Hi Level Duration</td>
<td></td>
<td>4</td>
<td>25</td>
<td>t_{los} ns</td>
<td></td>
</tr>
<tr>
<td>1003</td>
<td>t_MASL</td>
<td>Clock Signal Lo Level Duration</td>
<td></td>
<td>4</td>
<td>25</td>
<td>t_{los} ns</td>
<td></td>
</tr>
<tr>
<td>BiSS C Protocol</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1004</td>
<td>t_MAS</td>
<td>Permissible Clock Period</td>
<td>t_{los} according to Table 34</td>
<td>5</td>
<td>100</td>
<td>2x t_{los} ns</td>
<td></td>
</tr>
<tr>
<td>1005</td>
<td>t_MASH</td>
<td>Clock Signal Hi Level Duration</td>
<td></td>
<td>5</td>
<td>25</td>
<td>t_{los} ns</td>
<td></td>
</tr>
<tr>
<td>1006</td>
<td>t_MASL</td>
<td>Clock Signal Lo Level Duration</td>
<td></td>
<td>5</td>
<td>25</td>
<td>t_{los} ns</td>
<td></td>
</tr>
</tbody>
</table>

Figure 3: Timing diagram in SSI protocol.

Figure 4: Timing diagram in BiSS C protocol.
PARAMETER and REGISTER

**Register Description, Overview**  .......... Page 10

**Signal Conditioning**  .................. Page 11

- **GAIN:** Gain Select
- **SINOFFS:** Offset Calibration Sine
- **COSOFFS:** Offset Calibration Cosine
- **REFOFFS:** Offset Calibration Reference
- **RATIO:** Amplitude Calibration
- **PHASE:** Phase Calibration

**Converter Function**  .................. Page 12

- **SELRES:** Resolution
- **HYS:** Hysteresis
- **FCTR:** Max. Permissible Converter Frequency

**Incremental Signals**  .................. Page 15

- **CFGABZ:** Output A, B, Z
- **ROT:** Direction of Rotation
- **CBZ:** 24-bit Period Counter Configuration
- **ENRESDEL:** Output Delay A, B, Z
- **ZPOS:** Zero Signal Position
- **CFGZ:** Zero Signal Length
- **CFGAB:** Zero Signal Logic

**Signal Monitoring and Error Messages**  .......... Page 17

- **SELAMPL:** Amplitude Monitoring, function
- **AMPL:** Amplitude Monitoring, thresholds
- **AERR:** Amplitude Error
- **FERR:** Frequency Error

**Test Functions**  ................ Page 18

- **TMODE:** Test Mode
- **TMA:** Analog Test Mode

**BISS Interface**  ................ Page 19

- **SELSSI:** Protocol Version
- **TIMO, TOA:** Timeout
- **TOS:** Timeout Short**
- **M2S:** Data Output and Options
- **CRC6:** CRC Polynomial and Status Messages
- **NZB:** Zero Bit
- **ENCDS:** Protocol Options
- **RPL:** Register Protection Settings
- **GRAY:** SSI Data Format

### Table 5: Register layout

<table>
<thead>
<tr>
<th>Addr</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>ENCD</td>
<td>M2S(1:0)</td>
<td>SELRES(4:0)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x01</td>
<td>HYS(2:0)</td>
<td>ZPOS(4:0)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x02</td>
<td>ENRESDEL</td>
<td>SELSSI</td>
<td>ROT</td>
<td>CBZ</td>
<td>CFGABZ(1:0)</td>
<td>CFGZ(1:0)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x03</td>
<td>CRC6</td>
<td>NZB</td>
<td>CFGAB(1:0)</td>
<td>RPL</td>
<td>0</td>
<td>AERR</td>
<td>FERR</td>
<td></td>
</tr>
<tr>
<td>0x04</td>
<td>-</td>
<td>FCTR(7:0)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x05</td>
<td>GRAY</td>
<td>-</td>
<td>FCTR(14:8)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x06</td>
<td>reserved*</td>
<td>TIMO</td>
<td>0</td>
<td>TMODE(2:0)</td>
<td>TMA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x07</td>
<td>reserved*</td>
<td>TOA</td>
<td>reserved*</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x08</td>
<td>GAIN(3:0)</td>
<td>SINOFFS(7:0)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x09</td>
<td>-</td>
<td>COSOFFS(7:0)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x0B</td>
<td>PHASE(5:0)</td>
<td>REFOFFS</td>
<td>RATIO(4)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x0C</td>
<td>reserved*</td>
<td>SELAMPL</td>
<td>AMPL(1:0)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x0D</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x0E</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x0F</td>
<td>CRC_E2P(7:0) - check value read from the EEPROM for addresses 0x00 to 0x0E</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x10 - 0x1F</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x41 - 0x7F</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Register contents are random when powering up without an EEPROM. When no register protection is active, all registers permit read and write access (see RPL).
*Reserved registers must be programmed to zero. **For TOS see table 42 on page 21.
Input stages SIN and COS are configured as instrumentation amplifiers. The amplifier gain must be selected in accordance with the input signal amplitude and programmed to register GAIN according to the following table. Half of the supply voltage is available at VREF as a center voltage to enable the DC level to be adapted.

<table>
<thead>
<tr>
<th>GAIN</th>
<th>Adr 0x08, Bit 7:4</th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Code</td>
<td>Amplitude</td>
<td>Sine/Cosine Input Signal Levels Vin()</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Differential</td>
<td>Single-ended</td>
<td>Differential</td>
<td>Single-ended</td>
</tr>
<tr>
<td>0x0F</td>
<td>80.000</td>
<td>up to 50 mVpp</td>
<td>up to 100 mVpp</td>
<td>0.7 V ... VDDA - 1.2 V</td>
<td>0.8 V ... VDDA - 1.2 V</td>
</tr>
<tr>
<td>0x0E</td>
<td>66.667</td>
<td>up to 60 mVpp</td>
<td>up to 120 mVpp</td>
<td>0.7 V ... VDDA - 1.2 V</td>
<td>0.8 V ... VDDA - 1.2 V</td>
</tr>
<tr>
<td>0x0D</td>
<td>53.333</td>
<td>up to 75 mVpp</td>
<td>up to 15 Vpp</td>
<td>0.7 V ... VDDA - 1.2 V</td>
<td>0.8 V ... VDDA - 1.2 V</td>
</tr>
<tr>
<td>0x0C</td>
<td>40.000</td>
<td>up to 0.12 Vpp</td>
<td>up to 0.24 Vpp</td>
<td>0.7 V ... VDDA - 1.2 V</td>
<td>1.3 V ... VDDA - 1.3 V</td>
</tr>
<tr>
<td>0x0B</td>
<td>33.333</td>
<td>up to 0.14 Vpp</td>
<td>up to 0.28 Vpp</td>
<td>0.7 V ... VDDA - 1.2 V</td>
<td>0.8 V ... VDDA - 1.3 V</td>
</tr>
<tr>
<td>0x0A</td>
<td>28.571</td>
<td>up to 0.15 Vpp</td>
<td>up to 0.3 Vpp</td>
<td>0.7 V ... VDDA - 1.2 V</td>
<td>1.3 V ... VDDA - 1.3 V</td>
</tr>
<tr>
<td>0x09</td>
<td>26.667</td>
<td>up to 0.15 Vpp</td>
<td>up to 0.4 Vpp</td>
<td>0.7 V ... VDDA - 1.2 V</td>
<td>0.8 V ... VDDA - 1.3 V</td>
</tr>
<tr>
<td>0x08</td>
<td>20.000</td>
<td>up to 0.28 Vpp</td>
<td>up to 0.56 Vpp</td>
<td>0.7 V ... VDDA - 1.2 V</td>
<td>1.4 V ... VDDA - 1.4 V</td>
</tr>
<tr>
<td>0x07</td>
<td>14.287</td>
<td>up to 0.4 Vpp</td>
<td>up to 0.8 Vpp</td>
<td>1.2 V ... VDDA - 1.3 V</td>
<td>1.4 V ... VDDA - 1.5 V</td>
</tr>
<tr>
<td>0x06</td>
<td>10.000</td>
<td>up to 0.5 Vpp</td>
<td>up to 1 Vpp</td>
<td>0.8 V ... VDDA - 1.4 V</td>
<td>1.0 V ... VDDA - 1.6 V</td>
</tr>
<tr>
<td>0x05</td>
<td>8.000</td>
<td>up to 0.6 Vpp</td>
<td>up to 1.2 Vpp</td>
<td>0.8 V ... VDDA - 1.4 V</td>
<td>1.1 V ... VDDA - 1.7 V</td>
</tr>
<tr>
<td>0x04</td>
<td>6.667</td>
<td>up to 0.75 Vpp</td>
<td>up to 1.5 Vpp</td>
<td>0.9 V ... VDDA - 1.5 V</td>
<td>1.3 V ... VDDA - 1.9 V</td>
</tr>
<tr>
<td>0x03</td>
<td>5.333</td>
<td>up to 0.75 Vpp</td>
<td>up to 2 Vpp</td>
<td>1.2 V ... VDDA - 1.6 V</td>
<td>1.7 V ... VDDA - 2.1 V</td>
</tr>
<tr>
<td>0x02</td>
<td>4.000</td>
<td>up to 1.2 Vpp</td>
<td>up to 2.4 Vpp</td>
<td>1.2 V ... VDDA - 1.7 V</td>
<td>1.8 V ... VDDA - 2.3 V</td>
</tr>
<tr>
<td>0x01</td>
<td>3.333</td>
<td>up to 1.5 Vpp</td>
<td>up to 3 Vpp</td>
<td>1.3 V ... VDDA - 1.8 V</td>
<td>2.0 V ... VDDA - 2.6 V</td>
</tr>
<tr>
<td>0x00</td>
<td>2.667</td>
<td>up to 1.5 Vpp</td>
<td>up to 3 Vpp</td>
<td>1.3 V ... VDDA - 1.8 V</td>
<td>2.0 V ... VDDA - 2.6 V</td>
</tr>
</tbody>
</table>

Table 6: Input gain

<table>
<thead>
<tr>
<th>SINOFFS</th>
<th>Adr 0x09, Bit 7:0</th>
<th>COSOFFS</th>
<th>Adr 0x0A, Bit 7:0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code</td>
<td>Output Offset</td>
<td>Input Offset</td>
<td></td>
</tr>
<tr>
<td>0x00</td>
<td>0 V</td>
<td>0 V</td>
<td></td>
</tr>
<tr>
<td>0x01</td>
<td>-7.8125 mV</td>
<td>-7.8125 mV / GAIN</td>
<td></td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
<td></td>
</tr>
<tr>
<td>0x7F</td>
<td>-0.9922 V</td>
<td>-0.9922 V / GAIN</td>
<td></td>
</tr>
<tr>
<td>0x80</td>
<td>0 V</td>
<td>0 V</td>
<td></td>
</tr>
<tr>
<td>0x81</td>
<td>+7.8125 mV</td>
<td>+7.8125 mV / GAIN</td>
<td></td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
<td></td>
</tr>
<tr>
<td>0xFF</td>
<td>+0.9922 V</td>
<td>+0.9922 V / GAIN</td>
<td></td>
</tr>
</tbody>
</table>

Notes: *) With REFOFFS = 0x00 and VDDA = 5 V.

Table 7: Sine/cosine offset calibration

<table>
<thead>
<tr>
<th>REFOFFS</th>
<th>Adr 0x0B, Bit 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code</td>
<td>Reference Voltage</td>
</tr>
<tr>
<td>0x00</td>
<td>Dependent on VDDA (example of application: MR sensors)</td>
</tr>
<tr>
<td>0x01</td>
<td>Not dependent on VDDA (example of application: Sin/Cos encoders)</td>
</tr>
</tbody>
</table>

Table 8: Offset reference

<table>
<thead>
<tr>
<th>RATIO</th>
<th>Adr 0x0B, Bit 0, Adr 0x08, Bit 3:0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code</td>
<td>COS / SIN</td>
</tr>
<tr>
<td>0x00</td>
<td>1.0000</td>
</tr>
<tr>
<td>0x01</td>
<td>1.0067</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>0xFF</td>
<td>1.1</td>
</tr>
</tbody>
</table>

Table 9: Amplitude calibration

<table>
<thead>
<tr>
<th>PHASE</th>
<th>Adr 0x0B, Bit 7:2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code</td>
<td>Phase Shift</td>
</tr>
<tr>
<td>0x00</td>
<td>90°</td>
</tr>
<tr>
<td>0x01</td>
<td>90.703125°</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>0x12</td>
<td>102.65625°</td>
</tr>
<tr>
<td>...</td>
<td>77.34375°</td>
</tr>
<tr>
<td>0x1F</td>
<td>102.65625°</td>
</tr>
</tbody>
</table>

Table 10: Phase calibration
### CONVERTER FUNCTIONS

#### SELRES

<table>
<thead>
<tr>
<th>Code</th>
<th>Binary Resolutions</th>
<th>Examples of Permissible Input Frequencies $f_{\text{in}}^{\text{max}}$ (FCTR 0x0004, 0x4302)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>0x01</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>0x02</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>0x03</td>
<td>8192</td>
<td>171 Hz, 1.14 kHz</td>
</tr>
<tr>
<td>0x04</td>
<td>4096</td>
<td>342 Hz, 2.28 kHz</td>
</tr>
<tr>
<td>0x05</td>
<td>2048</td>
<td>683 Hz, 4.56 kHz</td>
</tr>
<tr>
<td>0x06</td>
<td>1024</td>
<td>1.37 kHz, 9.1 kHz</td>
</tr>
<tr>
<td>0x07</td>
<td>512</td>
<td>2.73 kHz, 18.2 kHz</td>
</tr>
<tr>
<td>0x08</td>
<td>256</td>
<td>5.47 kHz, 36.5 kHz</td>
</tr>
<tr>
<td>0x09</td>
<td>128</td>
<td>10.9 kHz, 72.9 kHz</td>
</tr>
<tr>
<td>0x0A</td>
<td>64</td>
<td>21.9 kHz, 145.8 kHz</td>
</tr>
<tr>
<td>0x0B</td>
<td>32</td>
<td>43.7 kHz (max. 250 kHz)</td>
</tr>
<tr>
<td>0x0C</td>
<td>16</td>
<td>87.5 kHz (max. 250 kHz)</td>
</tr>
<tr>
<td>0x0D</td>
<td>8</td>
<td>175 kHz (max. 250 kHz)</td>
</tr>
<tr>
<td>0x0E</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>0x0F</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Table 11: Binary resolutions

#### SELRES

<table>
<thead>
<tr>
<th>Code</th>
<th>Decimal Resolutions</th>
<th>Examples of Permissible Input Frequencies $f_{\text{in}}^{\text{max}}$ (FCTR 0x0004, 0x4302)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x10</td>
<td>2000</td>
<td>700 Hz, 4.67 kHz</td>
</tr>
<tr>
<td>0x11</td>
<td>1600</td>
<td>875 Hz, 5.83 kHz</td>
</tr>
<tr>
<td>0x12</td>
<td>1000</td>
<td>1.4 kHz, 9.33 kHz</td>
</tr>
<tr>
<td>0x13</td>
<td>800</td>
<td>1.75 kHz, 11.67 kHz</td>
</tr>
<tr>
<td>0x14</td>
<td>500</td>
<td>2.8 kHz, 18.67 kHz</td>
</tr>
<tr>
<td>0x15</td>
<td>400</td>
<td>3.5 kHz, 23.3 kHz</td>
</tr>
<tr>
<td>0x16</td>
<td>250</td>
<td>5.6 kHz, 37.3 kHz</td>
</tr>
<tr>
<td>0x17</td>
<td>125</td>
<td>5.6 kHz, 37.3 kHz</td>
</tr>
<tr>
<td>0x18</td>
<td>320</td>
<td>4.4 kHz, 29.2 kHz</td>
</tr>
<tr>
<td>0x19</td>
<td>160</td>
<td>4.4 kHz, 29.2 kHz</td>
</tr>
<tr>
<td>0x1A</td>
<td>80</td>
<td>4.4 kHz, 29.2 kHz</td>
</tr>
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<td>0x1B</td>
<td>40</td>
<td>4.4 kHz, 29.2 kHz</td>
</tr>
<tr>
<td>0x1C</td>
<td>200</td>
<td>7.0 kHz, 46.7 kHz</td>
</tr>
<tr>
<td>0x1D</td>
<td>100</td>
<td>7.0 kHz, 46.7 kHz</td>
</tr>
<tr>
<td>0x1E</td>
<td>50</td>
<td>7.0 kHz, 46.7 kHz</td>
</tr>
<tr>
<td>0x1F</td>
<td>25</td>
<td>7.0 kHz, 46.7 kHz</td>
</tr>
</tbody>
</table>

Notes

*) Not suitable for incremental output on A, B.

*2,4,8 The internal resolution is higher by a factor of 2, 4 or 8.

Table 12: Decimal resolutions

#### HYS

<table>
<thead>
<tr>
<th>Code</th>
<th>Hysteresis in degrees</th>
<th>Hysteresis in LSB</th>
<th>Absolute error*</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>0°</td>
<td>1 LSB @ 12bit</td>
<td>0.044°</td>
</tr>
<tr>
<td>0x01</td>
<td>0.0879°</td>
<td>1/2 LSB @ 10bit</td>
<td>0.088°</td>
</tr>
<tr>
<td>0x02</td>
<td>0.1758°</td>
<td>1 LSB @ 10bit</td>
<td>0.176°</td>
</tr>
<tr>
<td>0x03</td>
<td>0.3516°</td>
<td>1/2 LSB @ 10bit</td>
<td>0.352°</td>
</tr>
<tr>
<td>0x04</td>
<td>0.7031°</td>
<td>1 LSB @ 10bit</td>
<td>0.703°</td>
</tr>
<tr>
<td>0x05</td>
<td>1.4063°</td>
<td>1 LSB @ 10bit</td>
<td>1.406°</td>
</tr>
<tr>
<td>0x06</td>
<td>5.625°</td>
<td>only recommended for calibration</td>
<td></td>
</tr>
<tr>
<td>0x07</td>
<td>45°</td>
<td>only recommended for calibration</td>
<td></td>
</tr>
</tbody>
</table>

Notes

*) The resulting absolute error is equivalent to half the angle hysteresis.

Table 13: Hysteresis
The converter frequency automatically adjusts to the value required by the input frequency and resolution. This value ranges from zero to a maximum dependent on the oscillator frequency that is set via register FCTR.

**Serial Data Output**

For BiSS or SSI output the maximum possible converter frequency can be adjusted to suit the maximum input frequency; an automatic converter resolution step-down feature can be enabled via the FCTR register. Should the input frequency exceed the frequency limit of the selected converter resolution, the LSB is kept stable and not resolved any further; the interpolation resolution halves.

If the next frequency limit is overshot, the LSB and LSB +1 are kept stable and so on. If the input frequency again sinks below this frequency threshold, fine resolution automatically returns.

With the programming of CRC6 = 1 a resolution step-down will be signalled via the BiSS warning bit.

### Max. Possible Converter Frequency for Serial Data Output

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0004</td>
<td>X X X X</td>
<td>BiSS</td>
<td>fosc(min) / 40 / Resolution</td>
<td>–</td>
<td>0.17 0.5 7.0</td>
</tr>
<tr>
<td>0x4102</td>
<td>≥ 8 X X X</td>
<td>BISS</td>
<td>fosc(min) / 24 / Resolution</td>
<td>Rel. angle error 2x increased</td>
<td>0.28 2.3 11.7</td>
</tr>
<tr>
<td>0x4202</td>
<td>≥ 16 X X X</td>
<td>BISS</td>
<td>2 x fosc(min) / 24 / Res.</td>
<td>Rel. angle error 4x increased</td>
<td>0.57 4.6 23.3</td>
</tr>
<tr>
<td>0x4302</td>
<td>≥ 32 X X X</td>
<td>BISS</td>
<td>4 x fosc(min) / 24 / Res.</td>
<td>Rel. angle error 8x increased</td>
<td>1.14 9.1 46.7</td>
</tr>
<tr>
<td>0x4702</td>
<td>≥ 64 X - X</td>
<td>BISS</td>
<td>8 x fosc(min) / 24 / Res.</td>
<td>Resolution lowered by factor of 2</td>
<td>2.3 18.2 -</td>
</tr>
<tr>
<td>0x4B02</td>
<td>≥ 128 X - X</td>
<td>BISS</td>
<td>16 x fosc(min) / 24 / Res.</td>
<td>Res. lowered by factor of 2-4</td>
<td>4.6 36.5 -</td>
</tr>
<tr>
<td>0x4F02</td>
<td>≥ 256 X - X</td>
<td>BISS</td>
<td>32 x fosc(min) / 24 / Res.</td>
<td>Res. lowered by factor of 2-8</td>
<td>9.1 72.9 -</td>
</tr>
<tr>
<td>0x5302</td>
<td>≥ 512 X - X</td>
<td>BISS</td>
<td>64 x fosc(min) / 24 / Res.</td>
<td>Res. lowered by factor of 2-16</td>
<td>18.2 146 -</td>
</tr>
<tr>
<td>0x5702</td>
<td>≥ 1024 X - X</td>
<td>BISS</td>
<td>128 x fosc(min) / 24 / Res.</td>
<td>Res. lowered by factor of 2-32</td>
<td>36.5 250 -</td>
</tr>
<tr>
<td>0x5B02</td>
<td>≥ 2048 X - X</td>
<td>BISS</td>
<td>256 x fosc(min) / 24 / Res.</td>
<td>Res. lowered by factor of 2-64</td>
<td>72.9 - -</td>
</tr>
<tr>
<td>0x5F02</td>
<td>≥ 4096 X - X</td>
<td>BISS</td>
<td>512 x fosc(min) / 24 / Res.</td>
<td>Res. lowered by factor of 2-128</td>
<td>146 - -</td>
</tr>
<tr>
<td>0x6302</td>
<td>8192 X - X</td>
<td>BISS</td>
<td>1024 x fosc(min) / 24 / Res.</td>
<td>Res. lowered by factor of 2-256</td>
<td>250 - -</td>
</tr>
</tbody>
</table>

Notes *) Calculated with fosc(min) taken from Electrical Characteristics, item A02.

Table 14: Maximum converter frequency for serial data output.
Incremental Output to A, B and Z

Settings for the maximum possible converter frequency using register FCTR are governed by two criteria:

1. The maximum input frequency
2. System restrictions caused by slow counters or data transmission via cable

In this case it is sensible to preselect a minimum transition distance for the output signals. These settings also make a suitable zero-delay digital glitch filter that acts on ESD impact on the sensor and keeps the output signals spike free through temporal separation, for example.

Serial data output is possible at any time in BiSS or SSI protocol. However, for the transfer of angle data to the output register the incremental output is halted for one period of the clock signal at pin MA.

### Table 15: Maximum possible converter frequency for incremental A/B/Z output, defined by the maximum input frequency

<table>
<thead>
<tr>
<th>FCTR</th>
<th>Output Frequency fout @ ( f_{\text{fin}}^\text{max} ) A, B</th>
<th>Resolution Requirement at high input frequency fout 4 / fin( f_{\text{fs}}^\text{min} ) / Resolution</th>
<th>Restrictions at high input frequency fout 4 / fin( f_{\text{fs}}^\text{min} ) / Resolution</th>
<th>Examples* fout 4 / fin( f_{\text{fs}}^\text{min} ) [kHz] at resol.</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0004</td>
<td>325 kHz</td>
<td>X X fout 4 / fin( f_{\text{fs}}^\text{min} ) / Resolution</td>
<td>None</td>
<td>0.17 1.37 7.0</td>
</tr>
<tr>
<td>0x4102</td>
<td>542 kHz</td>
<td>X X fout 4 / fin( f_{\text{fs}}^\text{min} ) / Resolution</td>
<td>Relative angle error 2x increased</td>
<td>0.28 2.3 11.7</td>
</tr>
<tr>
<td>0x4202</td>
<td>1.08 MHz</td>
<td>X X 2 x fout 4 / fin( f_{\text{fs}}^\text{min} ) / Resolution</td>
<td>Relative angle error 4x increased</td>
<td>0.57 4.6 23.3</td>
</tr>
<tr>
<td>0x4302</td>
<td>2.17 MHz</td>
<td>X X 4 x fout 4 / fin( f_{\text{fs}}^\text{min} ) / Resolution</td>
<td>Relative angle error 8x increased</td>
<td>1.14 9.1 46.7</td>
</tr>
</tbody>
</table>

Notes *) Calculated with fout 4 / fin\( f_{\text{fs}}^\text{min} \) taken from Electrical Characteristics, item A02.

### Table 16: Maximum possible converter frequency for incremental A/B/Z output, defined by the minimum transition distance

<table>
<thead>
<tr>
<th>FCTR</th>
<th>Output Frequency fout @ ( t_{\text{MTD}}^\text{max} ) A, B</th>
<th>Resolution Requirement at high input frequency fout 4 / tMD</th>
<th>Restrictions at high input frequency fout 4 / tMD</th>
<th>Example* fout 4 / tMD [µsec]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00FF</td>
<td>11.2 kHz</td>
<td>X X 2048 / fout 4 / tMD</td>
<td>None</td>
<td>22.3</td>
</tr>
<tr>
<td>0x00FE</td>
<td>11.27 kHz</td>
<td>X X 2040 / fout 4 / tMD</td>
<td>None</td>
<td>22.2</td>
</tr>
<tr>
<td>0x00FD</td>
<td>11.3 kHz</td>
<td>X X 2032 / fout 4 / tMD</td>
<td>None</td>
<td>22.1</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>0x0006</td>
<td>411 kHz</td>
<td>X X 56 / fout 4 / tMD</td>
<td>None</td>
<td>0.61</td>
</tr>
<tr>
<td>0x0005</td>
<td>479 kHz</td>
<td>X X 48 / fout 4 / tMD</td>
<td>None</td>
<td>0.52</td>
</tr>
<tr>
<td>0x0004</td>
<td>575 kHz</td>
<td>X X 40 / fout 4 / tMD</td>
<td>None</td>
<td>0.43</td>
</tr>
<tr>
<td>0x4102</td>
<td>958 kHz</td>
<td>X X 24 / fout 4 / tMD</td>
<td>Relative angle error 2x increased</td>
<td>0.26</td>
</tr>
<tr>
<td>0x4202</td>
<td>1.92 MHz</td>
<td>X X 12 / fout 4 / tMD</td>
<td>Relative angle error 4x increased</td>
<td>0.13</td>
</tr>
<tr>
<td>0x4302</td>
<td>3.83 MHz</td>
<td>X X 6 / fout 4 / tMD</td>
<td>Relative angle error 8x increased</td>
<td>0.065</td>
</tr>
</tbody>
</table>

Notes *) Calculated with fout 4 / tMD taken from El.Char., item A02; transition distance output A vs. output B with same direction of rotation.
INCREMENTAL SIGNALS

<table>
<thead>
<tr>
<th>CFGABZ</th>
<th>Code</th>
<th>Mode</th>
<th>Pin A</th>
<th>Pin B</th>
<th>Pin Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>0x00</td>
<td>Normal</td>
<td>A</td>
<td>B</td>
<td>Z</td>
</tr>
<tr>
<td>0x01</td>
<td></td>
<td>Control signals for</td>
<td>CA</td>
<td>CB</td>
<td>CZ</td>
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<td></td>
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<td>external period</td>
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<td></td>
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<td>counters</td>
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<td>0x02</td>
<td>0x02</td>
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<td>CFGAB = 0x00</td>
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<td>AERR = 0x00</td>
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<td>Figure 5: Offset SIN*</td>
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<td>Figure 6: Offs. COS*</td>
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<td>Figure 7: Phase*</td>
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<td>AERR = 0x00</td>
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<tr>
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<td>Figure 8: Offset SIN*</td>
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<tr>
<td></td>
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<td>Figure 9: Offs. COS*</td>
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<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Figure 10: Amplit.*</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Notes</td>
<td></td>
<td>*) Trimmed accurately when duty cycle is 50%;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Recommended trimming order (after selecting GAIN): offset, phase, amplitude ratio, offset;</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 17: Outputs A, B, Z

<table>
<thead>
<tr>
<th>ROT</th>
<th>Code</th>
<th>Code direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>0x00</td>
<td>Ascending order, B then A</td>
</tr>
<tr>
<td>0x01</td>
<td>0x01</td>
<td>Descending order, A then B</td>
</tr>
</tbody>
</table>

Table 18: Code direction

<table>
<thead>
<tr>
<th>CBZ</th>
<th>Code</th>
<th>Reset via zero</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>0x00</td>
<td>Not activated</td>
</tr>
<tr>
<td>0x01</td>
<td>0x01</td>
<td>Activated</td>
</tr>
</tbody>
</table>

Table 19: Reset enable for period counter

<table>
<thead>
<tr>
<th>ENRESDEL</th>
<th>Code</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>0x00</td>
<td>immediately An external counter displays the absolute angle following power-on.</td>
</tr>
<tr>
<td>0x01</td>
<td>0x01</td>
<td>after 5 ms An external counter only displays changes vs. the initial power-on (conditional on standby at power-on)</td>
</tr>
</tbody>
</table>

Notes *) Output delay after device configuration and internal reset (A, B, Z remains on high).
### Table 21: Zero signal position

<table>
<thead>
<tr>
<th>Code</th>
<th>Position</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>0°</td>
</tr>
<tr>
<td>0x08</td>
<td>90°</td>
</tr>
<tr>
<td>0x10</td>
<td>180°</td>
</tr>
<tr>
<td>0x18</td>
<td>270°</td>
</tr>
<tr>
<td>0x01</td>
<td>11.25° (1 x 11.25°)</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>0x1F</td>
<td>348.75° (31 x 11.25°)</td>
</tr>
</tbody>
</table>

**Notes:** The zero signal is only output if released by the input pins (for instance with \( PZERO = 5 \) V, \( NZERO = VREF \)).

### Table 22: Zero signal length

<table>
<thead>
<tr>
<th>Code</th>
<th>Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>90°</td>
</tr>
<tr>
<td>0x01</td>
<td>180°</td>
</tr>
<tr>
<td>0x02..03</td>
<td>Synchronization</td>
</tr>
</tbody>
</table>

### Table 23: Zero signal logic

<table>
<thead>
<tr>
<th>Code</th>
<th>Z = 1 for</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>B = 1, A = 1</td>
</tr>
<tr>
<td>0x01</td>
<td>B = 0, A = 1</td>
</tr>
<tr>
<td>0x02</td>
<td>B = 1, A = 0</td>
</tr>
<tr>
<td>0x03</td>
<td>B = 0, A = 0</td>
</tr>
</tbody>
</table>

---

**Figure 12:** Incremental output signals for various zero signal lengths.

*Example gives a resolution of 64 (SELRES = 0x0A), a zero signal position of 45° (ZPOS = 0x04, CFGAB = 0x00) and no inversion of the direction of rotation (ROT = 0x00, COS leads SIN).*
### SIGNAL MONITORING and ERROR MESSAGES

**SELAMPL** 
Adr 0x0C, Bit 2

**AMPL** 
Adr 0x0C, Bit 1: 0

<table>
<thead>
<tr>
<th>Code</th>
<th>Voltage threshold $V_{th}$</th>
<th>Output amplitude*</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>0.60 x VDDA</td>
<td>1.4 Vpp</td>
</tr>
<tr>
<td>0x01</td>
<td>0.64 x VDDA</td>
<td>2.0 Vpp</td>
</tr>
<tr>
<td>0x02</td>
<td>0.68 x VDDA</td>
<td>2.6 Vpp</td>
</tr>
<tr>
<td>0x03</td>
<td>0.72 x VDDA</td>
<td>3.1 Vpp</td>
</tr>
</tbody>
</table>

**Sin² + Cos²** for SELAMPL = 1

<table>
<thead>
<tr>
<th>Code</th>
<th>$V_{limin}$ ↔ $V_{pmax}$</th>
<th>Output amplitude*</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x04</td>
<td>(0.20 ↔ 0.9) x VDDA</td>
<td>1.0 Vpp ↔ 4.5 Vpp</td>
</tr>
<tr>
<td>0x05</td>
<td>(0.30 ↔ 0.9) x VDDA</td>
<td>1.5 Vpp ↔ 4.5 Vpp</td>
</tr>
<tr>
<td>0x06</td>
<td>(0.40 ↔ 0.9) x VDDA</td>
<td>2.0 Vpp ↔ 4.5 Vpp</td>
</tr>
<tr>
<td>0x07</td>
<td>(0.50 ↔ 0.9) x VDDA</td>
<td>2.5 Vpp ↔ 4.5 Vpp</td>
</tr>
</tbody>
</table>

**Notes**
$V_{th}$, $V_{limin}$, $V_{pmax}$ are typical values; refer to Elec. Char. No. H01 cf. for maximal values.

*) Entries are calculated with VDDA = 5 V.

**Table 24: Signal amplitude monitoring**

**AERR** 
Adr 0x03, Bit 1

<table>
<thead>
<tr>
<th>Code</th>
<th>Amplitude error message</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>disabled</td>
</tr>
<tr>
<td>0x01</td>
<td>enabled</td>
</tr>
</tbody>
</table>

**Table 25: Amplitude error**

**FERR** 
Adr 0x03, Bit 0

<table>
<thead>
<tr>
<th>Code</th>
<th>Excessive frequency error message</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>disabled</td>
</tr>
<tr>
<td>0x01</td>
<td>enabled</td>
</tr>
</tbody>
</table>

**Notes**
Input frequency monitoring is operational for resolutions ≥ 16

**Table 26: Frequency error**

**Configuration error**

- Always enabled

**Table 27: Configuration error**

**Error Indication at NERR**

<table>
<thead>
<tr>
<th>Failure Mode</th>
<th>Pin signal NERR</th>
</tr>
</thead>
<tbody>
<tr>
<td>No error</td>
<td>HI</td>
</tr>
<tr>
<td>Amplitude error</td>
<td>LO/HI = 75 % (resp. HI for AERR = 0)</td>
</tr>
<tr>
<td>Frequency error</td>
<td>LO/HI = 50 % (resp. HI for FERR = 0)</td>
</tr>
<tr>
<td>Configuration</td>
<td>LO</td>
</tr>
<tr>
<td>Undervoltage</td>
<td>LO</td>
</tr>
<tr>
<td>System error</td>
<td>NERR = low caused by an external error signal</td>
</tr>
</tbody>
</table>

**Table 28: Error indication at NERR**

**Error Messages**

<table>
<thead>
<tr>
<th>Failure Mode</th>
<th>Error bits E1, E0 for BISS and SSI CRC6 = 0</th>
<th>Error bits nE, nW for BISS and SSI CRC6 = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>No error</td>
<td>1, 1</td>
<td>1, nW</td>
</tr>
<tr>
<td>Amplitude error</td>
<td>0, 1</td>
<td>0, nW</td>
</tr>
<tr>
<td>Frequency error</td>
<td>1, 0</td>
<td>0, nW</td>
</tr>
<tr>
<td>System error*</td>
<td>0, 0</td>
<td>0, nW</td>
</tr>
<tr>
<td>Warning**</td>
<td>—</td>
<td>nE, 0</td>
</tr>
</tbody>
</table>

*System error
**Warning

**Notes**
NERR pulled low by external signal
Automatic step-back of resolution
Data output is deactivated and SLO permanently high in case of: configuration phase, invalid configuration, undervoltage.

**Table 29: Error messages**

To enable the diagnosis of faults, the various types of error are signaled at NERR using a PWM code as given in the key on the left.

Two error bits are provided to enable communication via the I/O interface; these bits can decode four different types of error. If NERR is held at low by an external source, such as an error message from the system, for example, this can also be verified via the I/O interface.

Error are stored until the sensor data is output via the I/O interface and then deleted. Errors at NERR are displayed for a minimum of ca. 10 ms unless they are deleted beforehand by a data output.
If an error in amplitude occurs, conversion is terminated and the incremental output signals halted. An error in amplitude rules out the possibility of an error in frequency.

### TEST FUNCTIONS

#### TMODE

<table>
<thead>
<tr>
<th>Code</th>
<th>Signal at Z</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>Z</td>
<td>no test mode</td>
</tr>
<tr>
<td>0x01</td>
<td>A xor B</td>
<td>Output A EXOR B</td>
</tr>
<tr>
<td>0x02</td>
<td>ENCLK</td>
<td>iC-Haus device test</td>
</tr>
<tr>
<td>0x03</td>
<td>NLOCK</td>
<td>iC-Haus device test</td>
</tr>
<tr>
<td>0x04</td>
<td>CLK</td>
<td>iC-Haus device test</td>
</tr>
<tr>
<td>0x05</td>
<td>DIVC</td>
<td>iC-Haus device test</td>
</tr>
<tr>
<td>0x06</td>
<td>PZERO - NZERO</td>
<td>iC-Haus device test</td>
</tr>
<tr>
<td>0x07</td>
<td>TP</td>
<td>iC-Haus device test</td>
</tr>
</tbody>
</table>

Condition: CFGABZ = 0x00

#### TMA

<table>
<thead>
<tr>
<th>Code</th>
<th>Pin A</th>
<th>Pin B</th>
<th>Pin SDA</th>
<th>Pin SCL</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>A</td>
<td>B</td>
<td>SDA</td>
<td>SCL</td>
</tr>
<tr>
<td>0x01</td>
<td>COS+</td>
<td>COS-</td>
<td>SIN+</td>
<td>SIN-</td>
</tr>
</tbody>
</table>

Notes: To permit the verification of GAIN and OFFSET settings, signals are output after the input amplifier. A converter signal of 4 Vpp is the ideal here and should not be exceeded. Pin loads above 1 MΩ are advisable for accurate measurements.

EEPROM access is not possible during mode TMA.

Table 31: Analog test mode

The signal is set to ca. 4 Vpp using GAIN and must not be altered after calibration. Both display modes are suitable for OFFS (positive values) and RATIO adjustments; X/Y mode is preferable for PHASE. Test signals COS- (pin B) and SIN- (pin SCL) must be selected to set negative values for OFFS.

![Calibrated signals in TMA mode](image-url)
The serial I/O interface operates in BiSS C protocol mode and enables sensor data to be output in uninter ruptible cycles (data channel SCD). At the same time parameters can be exchanged via bidirectional register communication (data channel CD).

The sensor data produced by iC-NQC contains the angle value (S) with 3 to 13 bits, the period count (P) with 0, 8, 12 or 24 bits, two error bits (E1 and E0) and 5 or 6 CRC bits (CRC).

<table>
<thead>
<tr>
<th>Bits</th>
<th>Typ</th>
<th>Label</th>
</tr>
</thead>
<tbody>
<tr>
<td>0...24</td>
<td>DATA</td>
<td>Period counter P(23:0): 0, 8, 12, 24 bit (multiturn position)</td>
</tr>
<tr>
<td>3...13</td>
<td>DATA</td>
<td>Angle data S(12:0): 3 bis 13 bit (singleturn position)</td>
</tr>
<tr>
<td>1</td>
<td>ERROR</td>
<td>Error bit E1 (amplitude error)</td>
</tr>
<tr>
<td>1</td>
<td>ERROR</td>
<td>Error bit E0 (frequency error)</td>
</tr>
<tr>
<td>5...6</td>
<td>CRC</td>
<td>Polynomial 0x25 (x^5 + x^2 + x^0) (inverted bit output)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- oder -</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Polynomial 0x43 (x^6 + x^1 + x^0) (inverted bit output)</td>
</tr>
</tbody>
</table>

Table 32: BiSS data channels

**Table 33: Protocol version**

<table>
<thead>
<tr>
<th>SELSSI</th>
<th>ADR 0x02, Bit 6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code</td>
<td>Protocol</td>
</tr>
<tr>
<td>0</td>
<td>BiSS C</td>
</tr>
<tr>
<td>1</td>
<td>SSI</td>
</tr>
</tbody>
</table>

**Table 34: Timeout configuration (protectable)**

<table>
<thead>
<tr>
<th>TIMO</th>
<th>ADR 0x06, Bit 5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code</td>
<td>Clock</td>
</tr>
<tr>
<td>0</td>
<td>46-47</td>
</tr>
<tr>
<td>1</td>
<td>3-4</td>
</tr>
</tbody>
</table>

**Notes**
A ref. clock count is equal to \(\frac{32}{f_{osc}}\) (see Ele. Char., A02). The permissible max. clock frequency is specified by E06. *) A low clock frequency can reduce the permissible maximum input frequency since conversion is paused for one MA cycle from Latch onwards.

**Table 35: Period counter output**

<table>
<thead>
<tr>
<th>M2S</th>
<th>ADR 0x00, Bit 6:5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code</td>
<td>Data Length</td>
</tr>
<tr>
<td>0x00</td>
<td>-</td>
</tr>
<tr>
<td>0x01</td>
<td>P(7:0)</td>
</tr>
<tr>
<td>0x02</td>
<td>P(11:0)</td>
</tr>
<tr>
<td>0x03</td>
<td>P(23:0)</td>
</tr>
</tbody>
</table>

**Table 36: CRC Polynomial and status messages**

<table>
<thead>
<tr>
<th>CRC6</th>
<th>ADR 0x03, Bit 7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code</td>
<td>CRC Polynomial</td>
</tr>
<tr>
<td>0</td>
<td>determined by M2S</td>
</tr>
<tr>
<td>1</td>
<td>0x43</td>
</tr>
</tbody>
</table>
NZB

<table>
<thead>
<tr>
<th>Code</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Zero bit</td>
</tr>
<tr>
<td>1</td>
<td>No zero bit</td>
</tr>
</tbody>
</table>

Notes: The optional zero bit is output as the final bit after the CRC.

Table 37: Zero bit

ENCDS

<table>
<thead>
<tr>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>Data output BiSS B or SSI</td>
</tr>
<tr>
<td>0x01</td>
<td>Data output BiSS C</td>
</tr>
</tbody>
</table>

Table 38: Protocol options

M2S can be used to set the number of period counter bits sent as sensor data. The counter bits are transmitted before the angle value, with the MSB leading.

The 5-bit CRC output is based on polynomial 0x25 (100101b), with the 6-bit CRC output based on polynomial 0x43 (1000011b) automatically coming active with longer SCD data, or when preselected by CRC6. As a rule, CRC bits are sent inverted.

An additional zero bit can be output following the CRC bits. However, disabling the zero bit by NZB = 1 is recommended when the output data length does not need to comply with existing applications.

To obtain a position data output being compatible to the BiSS B protocol parameter ENCDS = 0 does switch off the CDS bit, without a replacement by a zero bit. Thus, the output data length is shortened by one bit and register communication is limited to the direction of the master to the slave. The bidirectional BiSS C register communication must be enabled by setting ENCDS = 1.

Example of BiSS Data Output

<table>
<thead>
<tr>
<th>SCD: Angle data</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bits</td>
</tr>
<tr>
<td>------</td>
</tr>
<tr>
<td>12</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>6</td>
</tr>
</tbody>
</table>

Config. SELRES = 0x04, M2S = 0x00, CRC6 = 1, NZB = 1

Table 39: Example format 1 for BiSS profile BP1

Register Communication

After the BiSS C protocol slave registers are directly addressed in a reserved address area (0x40 to 0x7F). Other storage areas are addressed dynamically and in blocks. BiSS addresses 0x00 to 0x3F aim for a register bank consisting of 64 bytes, the physical storage address of which is determined by Bank Select n.

iC-NQC supports up to 16 storage banks, making it possible to use an 8-bit EEPROM to its full capacity. There is therefore also enough storage space for an ID plate (EDS) and OEM data.

Information regarding memory map and addressing via BiSS is given on page 25).

Internal Reset Function

A write access at RAM address 0x00 (BiSS address 0x00 with Bank Select n = 0) triggers an internal reset.

Based on the current configuration in the RAM, iC-NQC restarts without reading the EEPROM. The configured interface timeout and write protect settings become active, the period counter is set to zero and any stored configuration errors are deleted. The data output via SLO and the incremental signals at A, B and Z are released. Providing no amplitude error is present, the converter again counts up from an angle value of zero to the current angle position.

Short BiSS Timeout

For programming via the I/O interface iC-NQC has a short BiSS timeout function according to the description of the BiSS C protocol (see page 19, Table 2, El. Char. no. 6).
Regardless of register protection settings a short time-out of typically 1.8 µs can be temporarily activated by writing value 0x07 to address 0x7C (address 124d). A controller can then transmit the device configuration over a shorter period.

The value written to address 0x7C is also transferred to the EEPROM, provided an EEPROM has been connected up and is available.

On reading address 0x7C the byte stored in the EEPROM is output as part of the BiSS device ID. Here, high-order bits 7:3 are part of the manufacturer's ID; low-order bits 2:0 act as an indicator of the timeout options (regular or short timeout, see Table 42).

<table>
<thead>
<tr>
<th>TOS</th>
<th>Function</th>
<th>Adr 0x7C, Bit 2:0</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>Regular timeout (configured by TIMO)</td>
<td>000 - Regular timeout (configured by TIMO)</td>
</tr>
<tr>
<td>001...111</td>
<td>Short timeout (equal to TIMO = 1)</td>
<td>001...111 - Short timeout (equal to TIMO = 1)</td>
</tr>
</tbody>
</table>

Table 42: Short timeout (via BiSS device ID)
I/O INTERFACE: SSI Protocol

iC-NQC can transmit position data in SSI protocol mode; the parameters described in the following give the necessary settings and options.

Table 43: Protocol version

<table>
<thead>
<tr>
<th>Code</th>
<th>Protocol</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>BiSS C</td>
</tr>
<tr>
<td>1</td>
<td>SSI</td>
</tr>
</tbody>
</table>

Figure 17: Example line signal (SSI)

Table 44: Timeout configuration for SSI

<table>
<thead>
<tr>
<th>Code</th>
<th>Timeout $t_{\text{loss}}$</th>
<th>fc(\text{MA})_{\text{min}}^{*}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Long: ca. 20 µs</td>
<td>50 kHz</td>
</tr>
<tr>
<td>1</td>
<td>not permitted</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Code</th>
<th>Additional bits</th>
<th>Ring operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>E1, E0</td>
<td>no</td>
</tr>
<tr>
<td>0</td>
<td>none</td>
<td>no</td>
</tr>
<tr>
<td>1</td>
<td>nE, nW, zero bit</td>
<td>yes</td>
</tr>
<tr>
<td>1</td>
<td>none</td>
<td>yes</td>
</tr>
</tbody>
</table>

Table 45: Period counter for SSI data output

<table>
<thead>
<tr>
<th>Code</th>
<th>Period counter output length</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>-</td>
</tr>
<tr>
<td>0x01</td>
<td>P(7:0)</td>
</tr>
<tr>
<td>0x02</td>
<td>P(11:0)</td>
</tr>
<tr>
<td>0x03</td>
<td>P(23:0)</td>
</tr>
</tbody>
</table>

Table 46: Options for SSI data output

<table>
<thead>
<tr>
<th>Code</th>
<th>SSI data format</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>binary coded</td>
</tr>
<tr>
<td>1</td>
<td>gray coded</td>
</tr>
</tbody>
</table>

Notes: Data output starts with MSB for binary or Gray coded data.

Table 47: SSI data format

<table>
<thead>
<tr>
<th>Code</th>
<th>SSI data format</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>binary coded</td>
</tr>
<tr>
<td>1</td>
<td>gray coded</td>
</tr>
</tbody>
</table>

Notes: Data output starts with MSB for binary or Gray coded data.

* A low clock frequency can reduce the permissible maximum input frequency since conversion is paused for one MA cycle from Latch onwards.
### Examples of SSI Data Output

#### SSI Output Formats

<table>
<thead>
<tr>
<th>Res</th>
<th>Mode</th>
<th>Error</th>
<th>CRC</th>
<th>T1</th>
<th>T2</th>
<th>T3</th>
<th>T4...</th>
<th>T10</th>
<th>T11</th>
<th>T12</th>
<th>T13</th>
<th>T14</th>
<th>T15</th>
<th>T16</th>
<th>T17</th>
<th>T18</th>
<th>T19</th>
<th>T20</th>
<th>T21</th>
<th>T22</th>
<th>T23</th>
<th>T24</th>
<th>T25</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 bit</td>
<td>SSI</td>
<td>X</td>
<td>-</td>
<td>S9</td>
<td>S8</td>
<td>S7</td>
<td>S6 ...</td>
<td>S0</td>
<td>E1</td>
<td>E0</td>
<td>0</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
</tr>
<tr>
<td>13 bit</td>
<td>SSI</td>
<td>*1</td>
<td>-</td>
<td>S12</td>
<td>S11</td>
<td>S10</td>
<td>S9 ...</td>
<td>S3</td>
<td>S2</td>
<td>S1</td>
<td>S0</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
</tr>
<tr>
<td></td>
<td>SSI-R</td>
<td>*2</td>
<td>-</td>
<td>S12</td>
<td>S11</td>
<td>S10</td>
<td>S9 ...</td>
<td>S3</td>
<td>S2</td>
<td>S1</td>
<td>S0</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
<td>Stop</td>
</tr>
<tr>
<td>25-bit SSI</td>
<td>SSI</td>
<td>X</td>
<td>-</td>
<td>P7</td>
<td>P6</td>
<td>P5</td>
<td>P4 ...</td>
<td>P0, S12, S11</td>
<td>S10</td>
<td>S9</td>
<td>S8</td>
<td>S7</td>
<td>S6</td>
<td>S5</td>
<td>S4</td>
<td>S3</td>
<td>S2</td>
<td>S1</td>
<td>S0</td>
<td>E1</td>
<td>E0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Configuration: Input SLI = 0, SELSSI = 1, M2S = 0x00, CRC6 = 0, NZB = 0, unless otherwise noted.

*1) CRC6 = 0, NZB = 1; *2) CRC6 = 1, NZB = 1; *3) M2S = 0x01

Caption: SSI = SSI protocol
SSI-R = SSI ring operation

Table 48: SSI transmission formats
EEPROM INTERFACE

The serial EEPROM interface consists of the two pins SCL and SDA and enables read and write access to a serial EEPROM with I²C interface (with at least 128 bytes, 5 V type with a 3.3 V function; e.g. 24C01, 24C02, 24C08 and maximal 24C16).

The configuration data in the EEPROM, of addresses 0x00 to 0x0F, is secured by a CRC check value to address 0x0F. When the device is powered up, the address range from 0x00 to 0x0F is mapped onto iC-NQC’s configuration RAM. The higher memory area contains BiSS C slave registers and optional memory banks available to the sensor system.

The register access to the configuration data and the memory banks 1 to 7 (intended for EDS) can be restricted by parameter RPL.

**N.B.** When writing configuration data to the EEPROM (BiSS addresses 0x10 to 0x1F) a wait time of at least 4 ms must be allowed after each register.

Example of CRC Calculation Routine

```c
unsigned char ucDataStream = 0;
int iCRCPoly = 0x127;
unsigned char ucCRC=0;
int i = 0;
ucCRC = 0; // start value !!!
for (iReg = 0; iReg<15; iReg ++)
{
    ucDataStream = ucGetValue(iReg);
    for (i=0; i<=7; i++)
    {
        if (((ucCRC & 0x80) != (ucDataStream & 0x80)))
            ucCRC = (ucCRC << 1) ^ iCRCPoly;
        else
            ucCRC = (ucCRC << 1);
        ucDataStream = ucDataStream << 1;
    }
}
```

Table 49: Check value for EEPROM data

<table>
<thead>
<tr>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>Check value formed by CRC polynomial 0x127</td>
</tr>
<tr>
<td>0xFF</td>
<td>Adr 0xFF, Bit 7:0</td>
</tr>
</tbody>
</table>

Table 50: Register overview

<table>
<thead>
<tr>
<th>RPL</th>
<th>Adr 0x03, Bit 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code</td>
<td>Bank 0 Config Dat.</td>
</tr>
<tr>
<td>0x00</td>
<td>read / write</td>
</tr>
<tr>
<td>0x1</td>
<td>-</td>
</tr>
</tbody>
</table>

Notes: *) Exception: write to 0x40 and 0x7C is always possible.
STARTUP BEHAVIOR

Startup With A Configured EEPROM
After the supply has been turned on (power-on reset), iC-NQC reads the configuration data from the EEPROM. During this phase it actively keeps error pin NERR at a low signal (open drain output), and data output SLO and the incremental signals at A, B and Z at a high signal.

After a successful CRC the data output to SLO and to the incremental A, B, and Z outputs is released and the error indication at pin NERR reset; an external pull-up resistor at pin NERR can supply a high signal. iC-NQC then switches to normal operation and determines the current angle position, providing that a sensor is connected up to it and there is no amplitude error (or this is deactivated).

Startup Without An EEPROM
The configuration RAM contains random values after startup; iC-NQC does not have a default configuration. Error pin NERR shows a low signal (open drain output); data output SLO and the incremental signals at A, B and Z indicate a high signal.

To reduce the device configuration time, a short timeout of 3 µs maximum (cf. TIMO = 1 and TOA = 0) can be temporarily activated by writing value 0x07 to address 0x7C (address 124d).

When operated without an EEPROM, iC-NQC does not respond to higher addresses - with the exception of the BiSS addresses reserved for manufacturer and device IDs (0x78 to 0x7F). This address area supplies the chip version from the ROM.

Initialization After Configuration Failure
So that it is always possible to talk to iC-NQC via the I/O interface, iC-NQC first ignores the register values of TIMO, TOA, RPL and TMA. Instead, iC-NQC applies the longest timeout (cf. TIMO = 0 and TOA = 0), ignores safety settings (cf. RPL = 0x0) and evaluates the BiSS register communication (CDM bit from the CD data channel).
During this phase regular bidirectional BiSS register communication is not yet possible, as data output SLO is permanently kept at high. Writing the configuration to RAM addresses 0x01 to 0x0C and to address 0x00 must be executed without evaluating a reply. Data input SLI is ignored; iC-NQC always uses slave ID 0.

Each cycle transmits a single bit only and can be reduced to four clocks plus the timeout (CDM). The following figures each show a single cycle with CDM = 0 and CDM = 1. A wide range of 100 ns to 12.5 µs is permissible for clock period T(MA); the timeout must last at least 30 µs.

A complete write cycle requires 14 cycles at CDM = 0 and a sequence of 32 cycles calculated according to BiSS-C register communication.

Notes: Data output SLO is only operational following initialization. The controller needs to execute the described initialization without any feedback (sending CDM bits without evaluating CDS bits).

N.B.: CDM bits are inverted on the line; when CDM = 1 the timeout is at low.

Programming tip: After writing a byte to the EEPROM the same byte should be read back. When doing so, iC-NQC does not output the start bit if the EEPROM is busy with its internal write procedure and so denies I2C access. Several read attempts may be required if the I2C interface is still blocked causing iC-NQC to refuse the read access. When writing to the EEPROM without reading the byte back, a wait time of at least 4 ms must be allowed after each register.
**Principle Input Circuits**

**Figure 22:** Input circuit for voltage signals of 1 Vpp with no ground reference. When ground is not separated the connection NSIN to VREF must be omitted.

**Figure 23:** Input circuit for current signals of 11 µA with no ground reference. Offset calibration is not possible with this circuit.

**Figure 24:** Input circuit for non-symmetrical voltage or current source signals with ground reference (adaptation via resistors R3, R4).

**Figure 25:** Simplified input wiring for non-symmetrical voltage signals with ground reference.

**Figure 26:** Input circuit for complementary low-side current source outputs, such as for optoencoder iC-WG.

**Figure 27:** Combined input circuit for 11 µA, 1 Vpp (with 120 Ω termination) or TTL encoder signals. RS3/4 and CS1 serve as protection against ESD and transients.
Input Circuit for Sine Encoders (1 Vpp)

**Figure 28:** Input circuit for sine encoders (0.8 Vpp to 1.2 Vpp) with 120Ω termination and low-pass filtering. R2/R3 serve as protection against ESD and transients, R4/R5 reduce the input signal to suit an input gain of 8.

Basic Circuit for MR Sensors

**Figure 29:** Basic circuit for the evaluation of MR bridge sensors.
EVALUATION BOARD

iC-NQC comes with a demo board for test purposes. Instructions are available separately.

DESIGN REVIEW: Function Notes

### iC-NQC 2

<table>
<thead>
<tr>
<th>No.</th>
<th>Function, Parameter/Code</th>
<th>Description and Application Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Please refer to datasheet release B1.</td>
</tr>
</tbody>
</table>

Table 52: Notes on chip functions regarding iC-NQC chip release 2.

### iC-NQC 3

<table>
<thead>
<tr>
<th>No.</th>
<th>Function, Parameter/Code</th>
<th>Description and Application Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GRAY</td>
<td>For Gray-coded data output clock cycles must be fully completed. An earlier termination results in invalid data for the following read out cycle.</td>
</tr>
<tr>
<td>2</td>
<td>Startup</td>
<td>An invalid CRC keeps only SLO permanently on high, the incremental output to A, B and Z is not blocked.</td>
</tr>
</tbody>
</table>

Table 53: Notes on chip functions regarding iC-NQC chip release 3.

### iC-NQC 5

<table>
<thead>
<tr>
<th>No.</th>
<th>Function, Parameter/Code</th>
<th>Description and Application Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GRAY</td>
<td>Gray-coded data output can be terminated at any time.</td>
</tr>
<tr>
<td>2</td>
<td>Startup</td>
<td>An invalid CRC keeps SLO and A, B and Z permanently on high (until an internal reset).</td>
</tr>
<tr>
<td>3</td>
<td>Period counting</td>
<td>Following power-on and after an internal reset the period counter is initialized with a value of zero (as all former chip releases). If an input angle of exactly 0° is applied and a movement towards 270° is following, the period counter counts to the value -1 (former chip releases maintain the value of zero).</td>
</tr>
</tbody>
</table>

Table 54: Notes on chip functions regarding iC-NQC chip release 5.

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<table>
<thead>
<tr>
<th>Type</th>
<th>Package</th>
<th>Order Designation</th>
</tr>
</thead>
<tbody>
<tr>
<td>iC-NQC</td>
<td>TSSOP20 4.4 mm</td>
<td>iC-NQC TSSOP20</td>
</tr>
<tr>
<td>Evaluation Board</td>
<td></td>
<td>iC-NQC EVAL NQ6D</td>
</tr>
</tbody>
</table>

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